IN THE SPECIFICATION

Please amend the specification as follows:

The paragraph beginning at page 5, line 28 is amended as follows:

In some embodiments, it is possible to fetch multiple basic blocks simultaneously, such as when trace cache 190 is included within processor 100. An example trace cache is described in US Patent No. 5,381,533, issued January 10, 1995 to Peleg, et al. entitled "Dynamic Flow Instruction Cache Memory Organized Around Trace Segments Independent Of Virtual Address Line." The Peleg example notwithstanding, the term "trace cache," as used herein, refers to any fetch structure that enables multiple basic blocks to be fetched in a single cycle. Because each trace cache entry provides information about the predicted future execution path, each trace cache entry can be augmented with trace hint information 192. For example, the execution path followed may influence whether rotation prediction should be performed or not, such as when two consecutive loop iterations are independent only when a certain condition is false. This information provides a value associated with each trace. Data dependence ~~checker~~ detector 114 is used to determine when the hint entry of a particular trace should be updated.